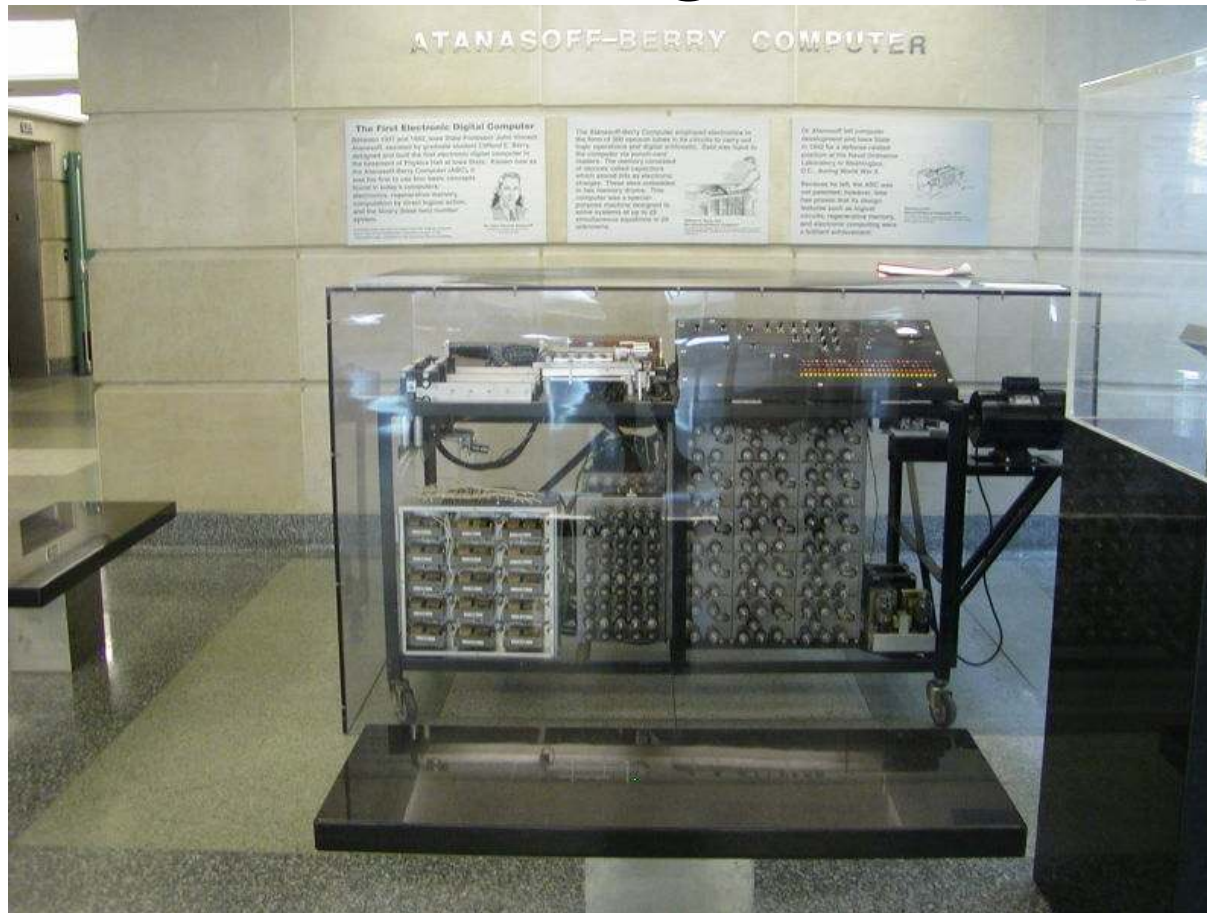# A law made to be broken

Historical and future challenges of semiconductor industry
-- with the focus on assembly process

Chuan Hu
Components Research /Intel Corp.

First electronic digital computer

- The **Atanasoff–Berry Computer** (**ABC**) : 320KG, Speed: 30 OPS. Built in 1942
  - Using binary digits to represent all numbers and data
  - Performing all calculations using electronics rather than wheels, ratchets, or mechanical switches
  - Organizing a system in which computation and memory are separated.

Chuan Hu/Intel 2008

Birth of modern computer:

- **2000 Nobel Prize in Physics:**
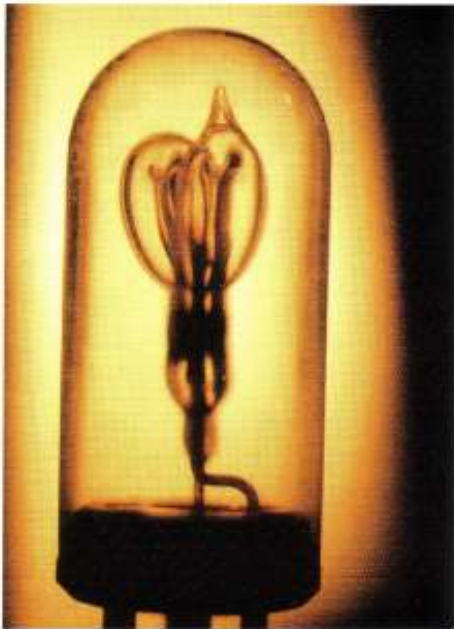 - **Jack St. Clair Kilby** "for his part in the invention of the integrated circuit"
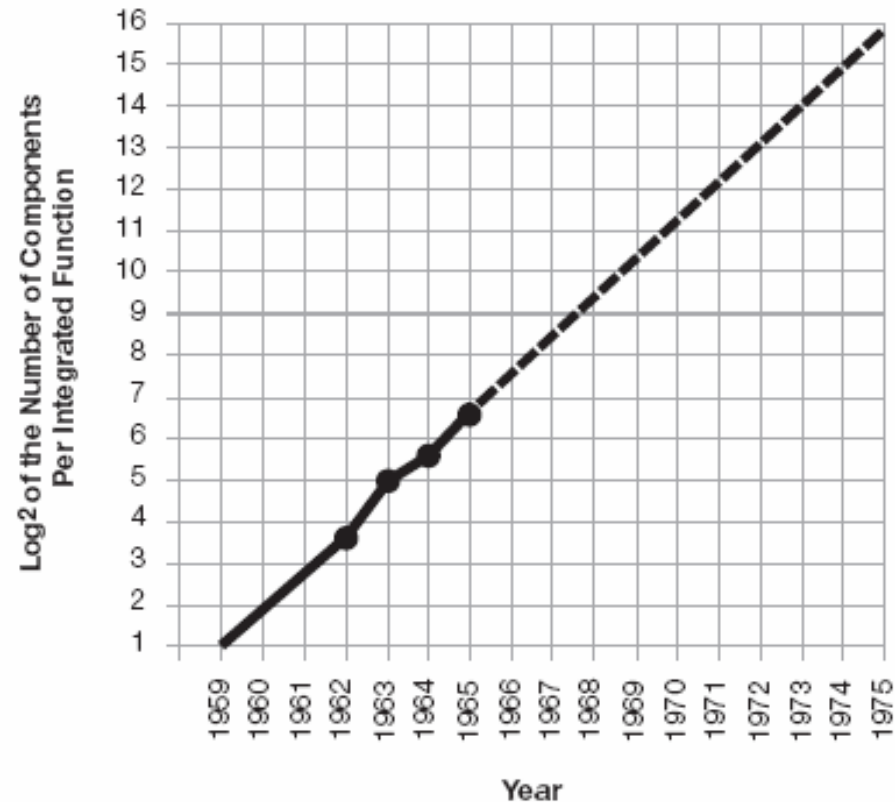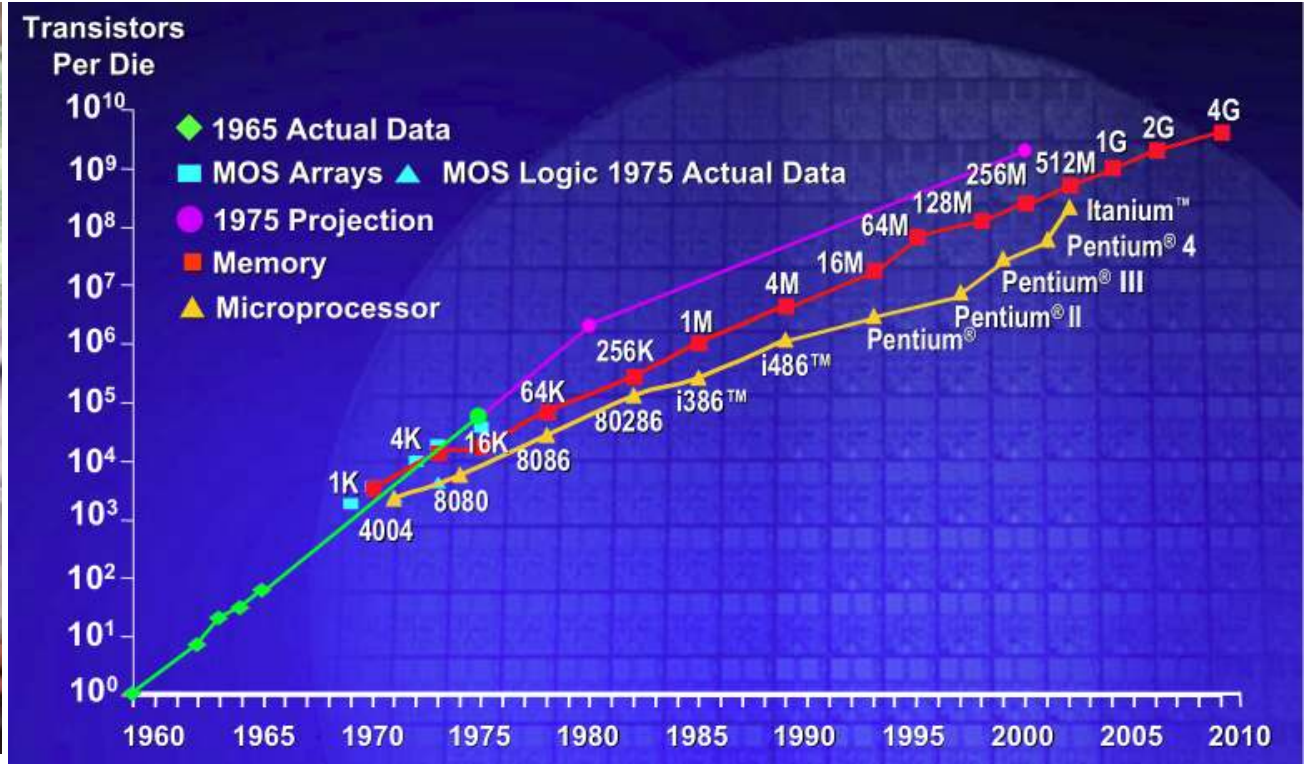

Figure 1. Vacuum tube.

Tube device

Semi-conductor transistor
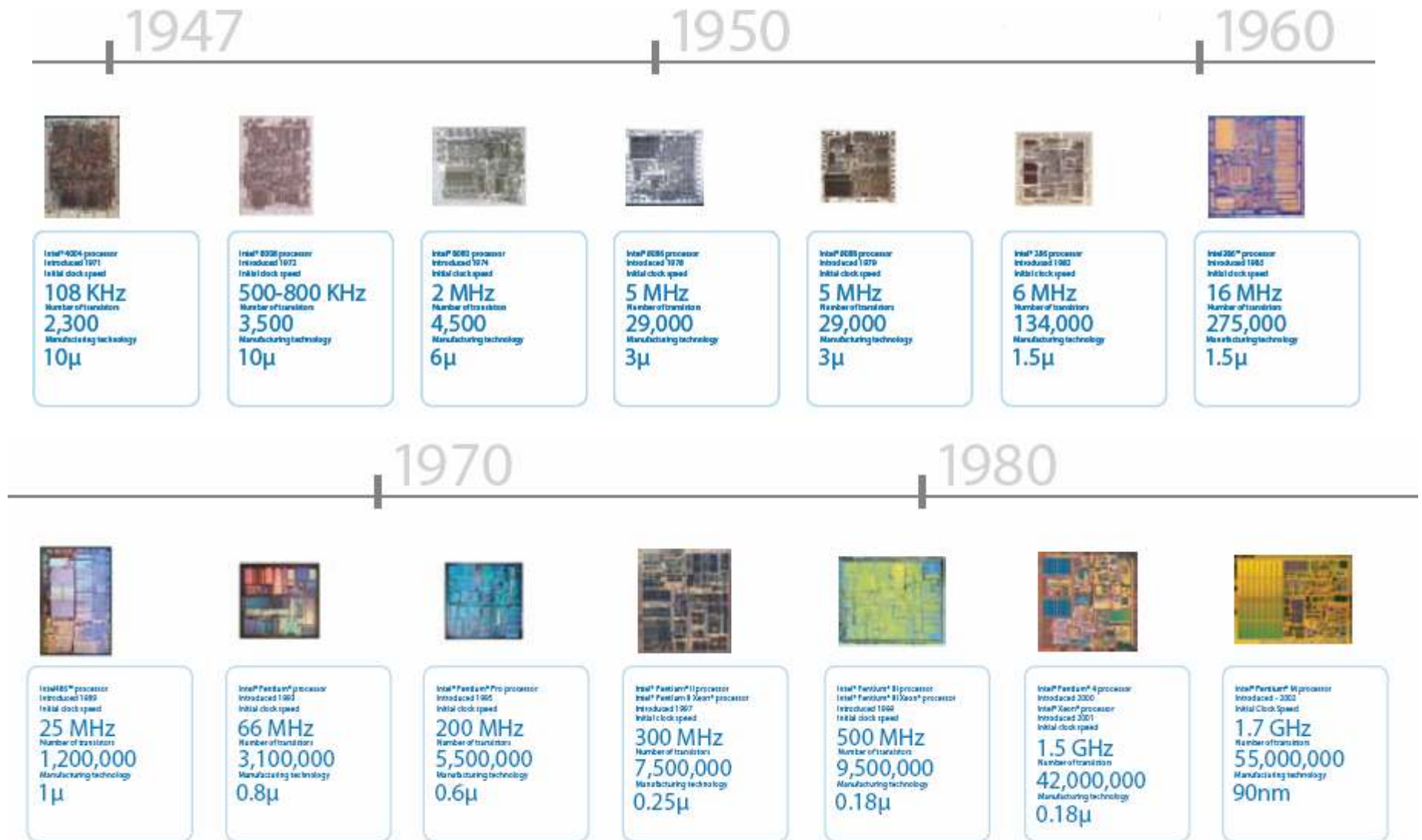
Moore's law in its original format

- Moore, Gordon E. (1965). "Cramming more components onto integrated circuits" 4. Electronics Magazine.
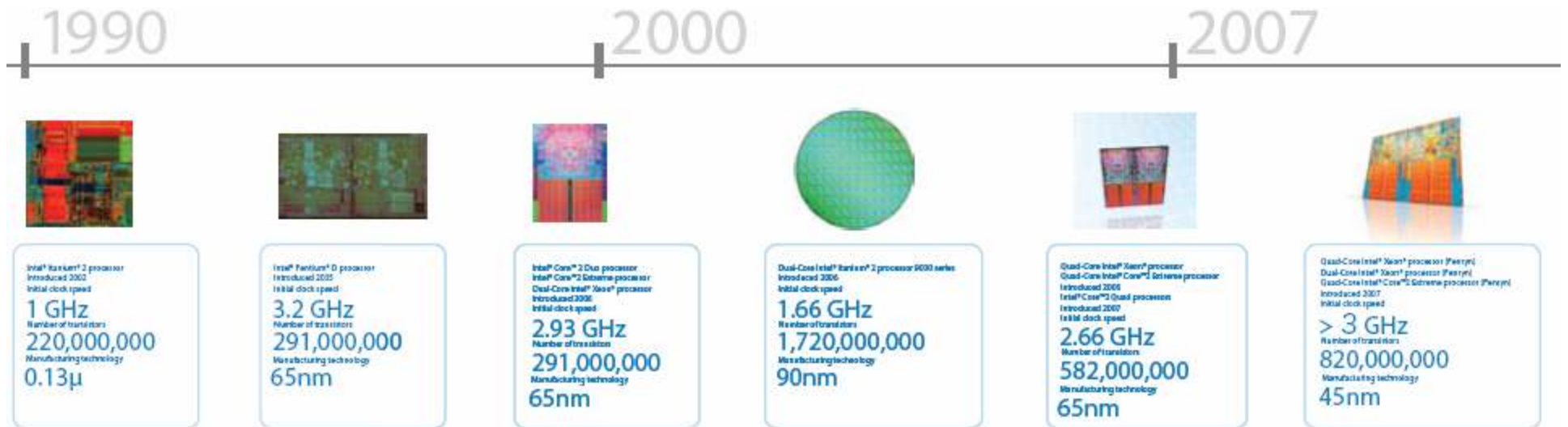
Moore's law:

- For how long?

Evolution of CPU: I

Chuan Hu/Intel 2008

6

Evolution of CPU: II

- 6 orders of magnitude faster than 60 years ago

Roadmap

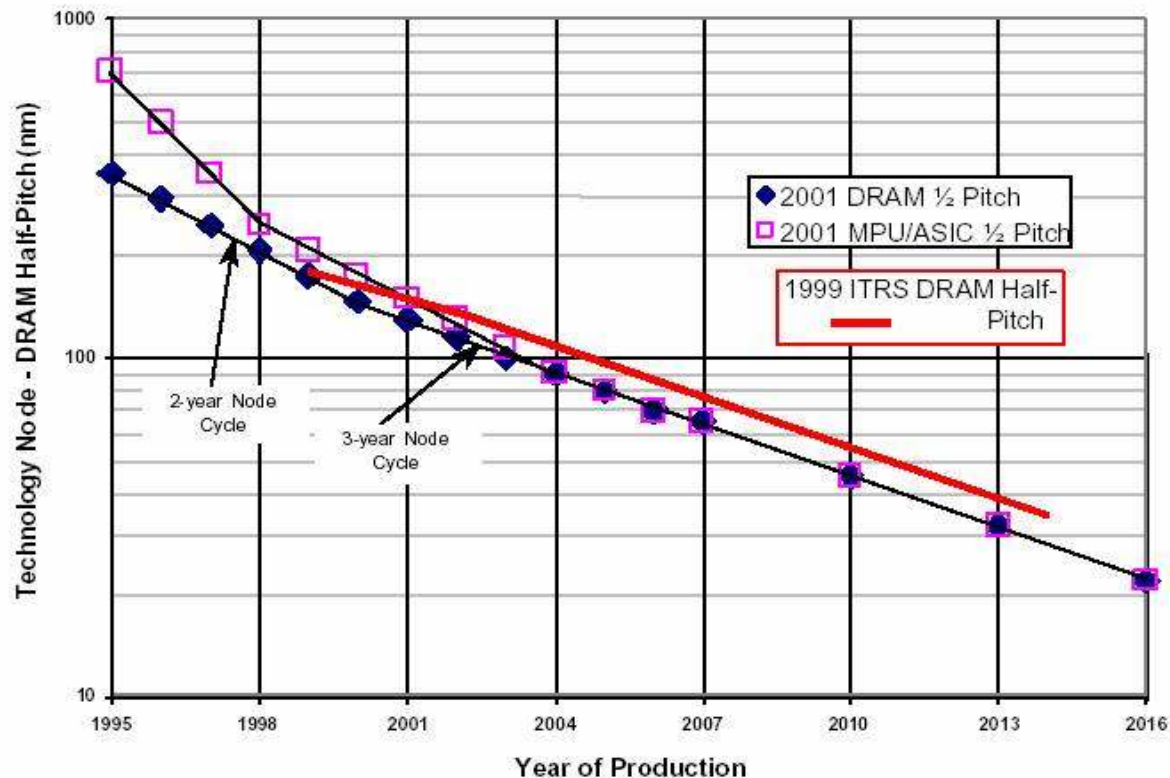**ITRS Roadmap Acceleration Continues...Half Pitch**

Figure 7 ITRS Roadmap Acceleration Continues—Half Pitch Trends

- In the foreseeable future, the semiconductor industry is still pursuing the Moore's law.

Chuan Hu/Intel 2008

Challenges: Lithography

ASML shipped the world's first EUV litho tool to SUNY Albany in 08/2006: $65M

Likely technology roadmap

half pitch		100	65	45	32	22	16	11
year		2005	2007	2009	2011	2013	2015
λ [nm]	NA							
248	0.80	0.32						
193	0.93		0.31					
	1.20		0.40	0.28				
	1.35			0.31	0.22	0.1		
	1.55				0.26	0.1		
13.5	0.25				0.41			
	0.35					0.57	0.41	
	0.45						0.53	0.37

Pitch relaxation or Double patterning

Low k$_1$ challenge

Fluid/ material challenge
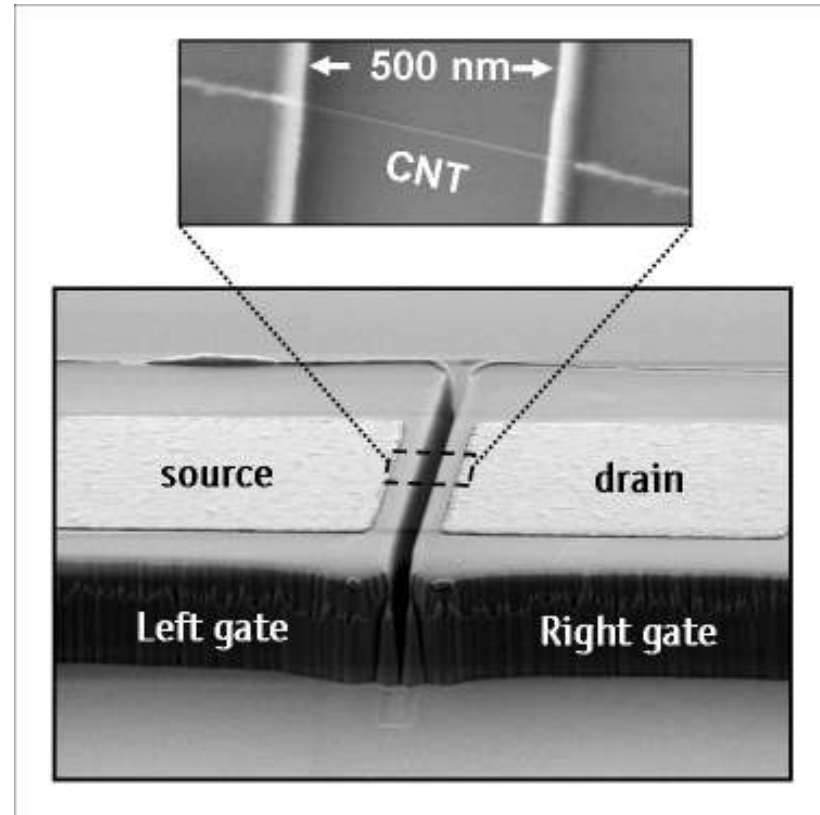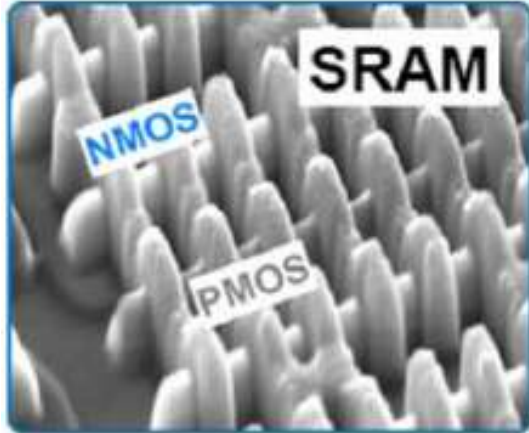
Infrastructure challenge

likely

opportunity

Arnold, ASML

- Extreme ultra violet lithography: mask to mounting
- Achievements: noncontact mask, subwave length litho: Immersion on going
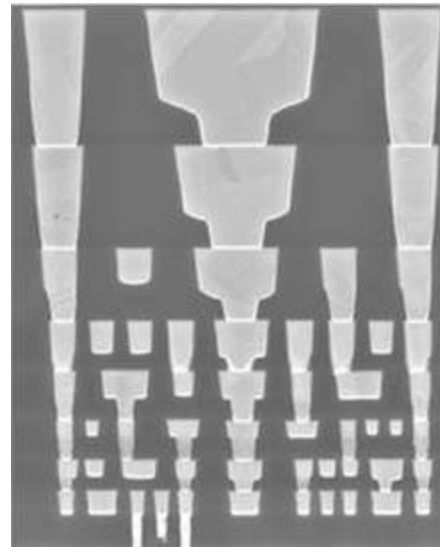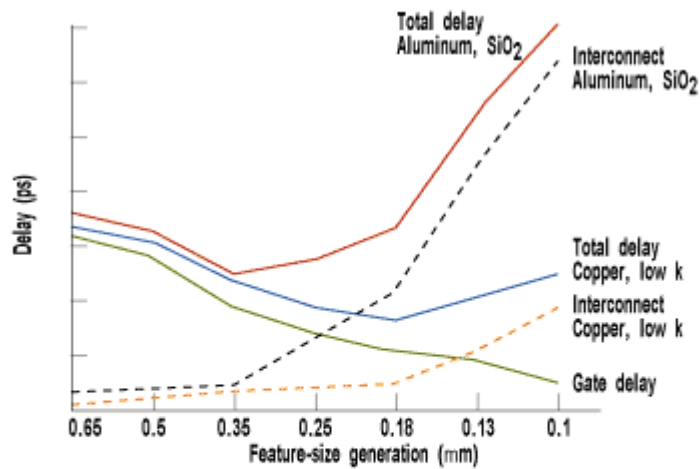
Challenges: transistors
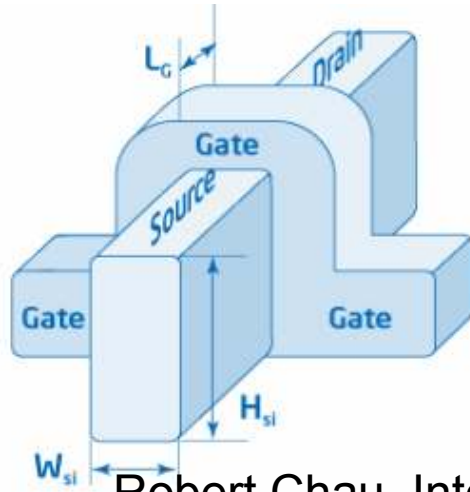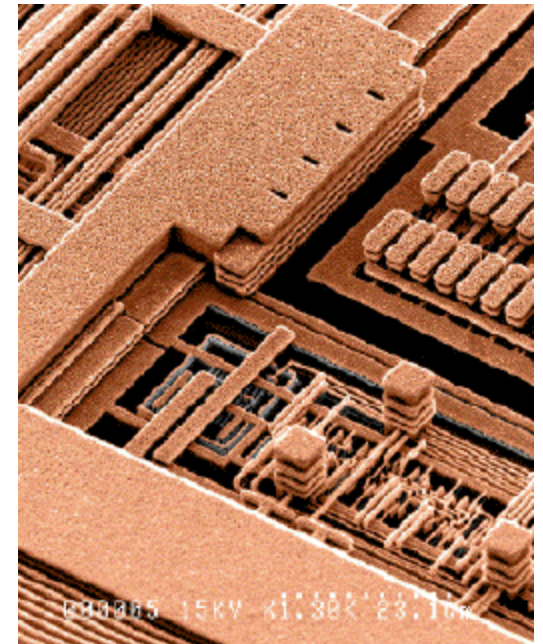

Robert Chau, Intel

Dan Ralph Cornell

- 3D transistor, (trigate, double gate), New transistor (CNT), quantum well, III/V, spintronics, hot electron reliability, leakage, quantum computing
- Achievements: Ion implantation/bipolar to CMOS/SOI/Metal gate, strained Si …

Chuan Hu/Intel 2008
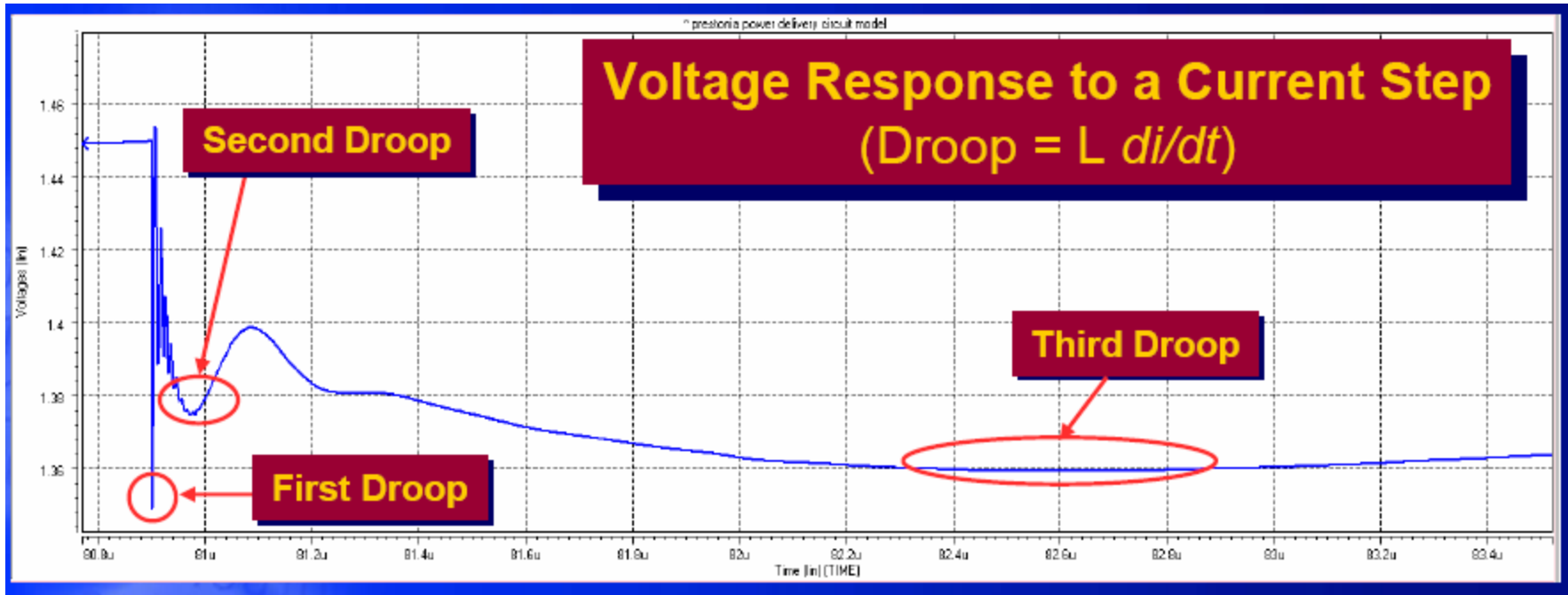
Challenges: interconnect

3. Gate delays at 100-nm line widths are secondary to those caused by copper wiring. The gap between the two expands beyond 100-nm IC feature sizes. (Source: Cadence Design Systems)

Intel's Cu/low k interconnect

IBM's Cu interconnect

- RC delay; CNT/nano wire interconnect; opto-interconnect: Si VESEL, waveguide, surface scattering …
- Achievements: CMP planarization/Cu metallization/low k dielectric

Chuan Hu/Intel 2008

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Challenges: packaging

- Power: delivery and heat removal: voltage scaling, energy efficient computing, power loss, thermal solutions
- Density: small pitch/solder ball, line width/space
- Multi-chip module/package
- Form factor: thin die, Stacked Si, SOP, SIP…
- Different packaging methods: wire bonding, BBUL…
- Wafer level packaging, Chip scale packaging…
- Integration with other advance technologies: biology, MEMS, quantum computing…
- IO/bandwidth: opto device, nano materials, flex…
- Environmental: leadfree solder, halogen free process…
- Reliability: solder, underfill, flux…
- Cost scaling: another interpretation of Moore's law is to bring more function with the same budget!

Power: power delivery

Voltage Response to a Current Step (Droop = L di/dt). Graph showing First Droop, Second Droop, and Third Droop on a voltage vs. time plot.
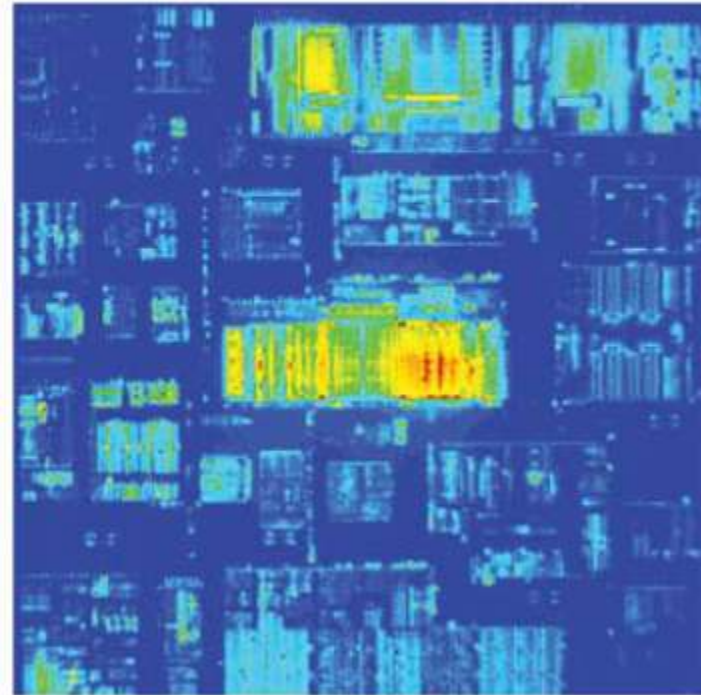
- Embedded passive: capacitor, inductor, other VR integrated close to transistors, fast VR…

Power: thermal

Intel Pentium® III Processor
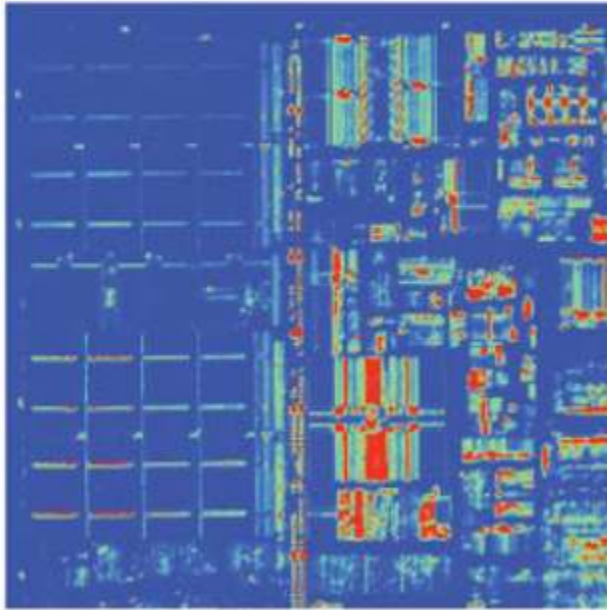
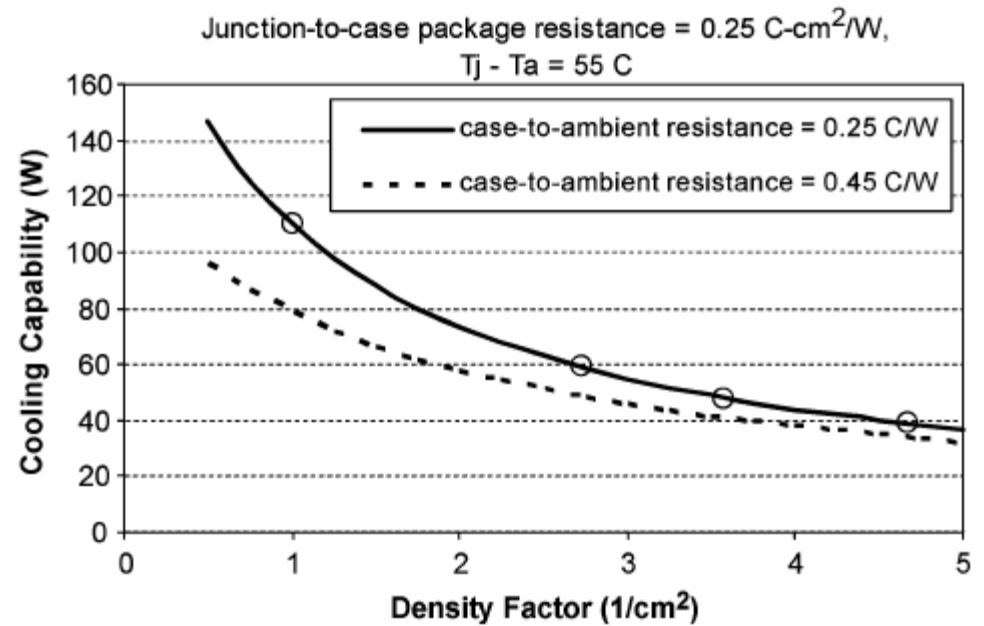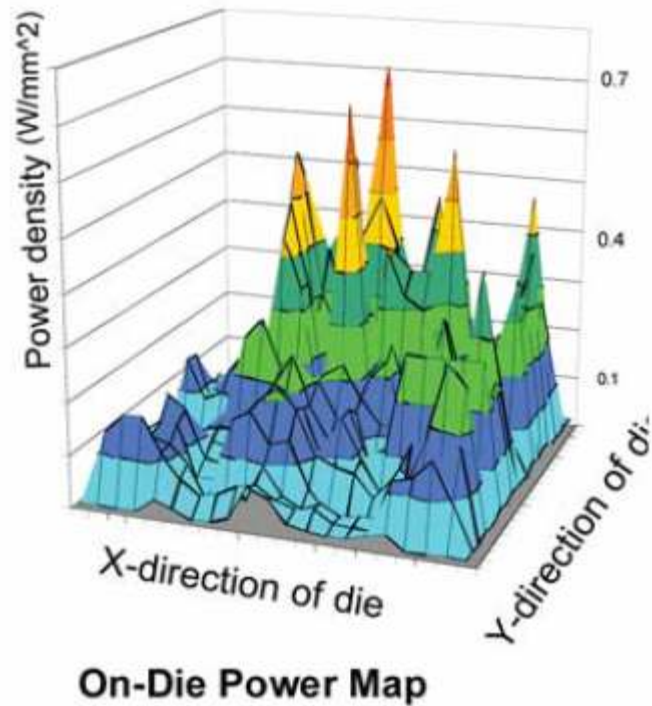Intel Itanium® Processor

IR image of power distribution.
Mahajan Intel

- Total power capped but hot spot still a big issue.

Chuan Hu/Intel 2008

Hotspot

Mahajan, Intel

- Cooling solutions become less effective when non-uniformity increases.
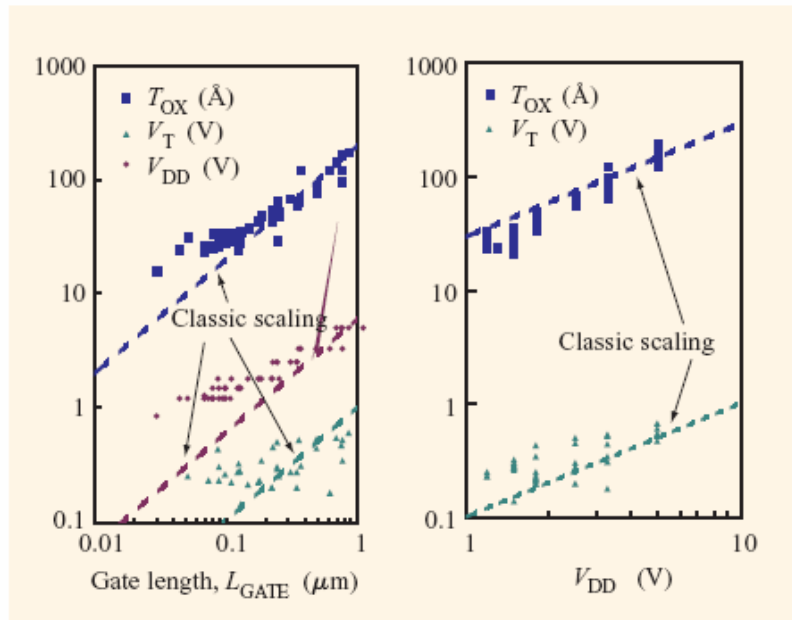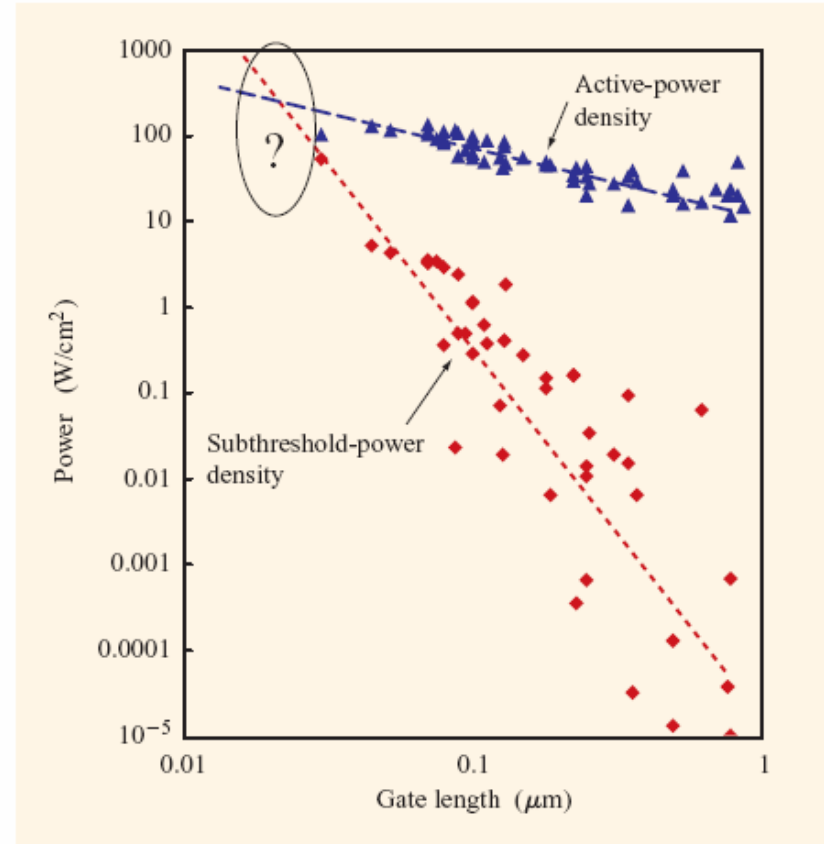
Power trend and scaling

Figure 1

Published industry trends (data points) are compared to "classic" scaling (dashed curves). V_T and V_{DD} show clear signs of deviation from classic scaling with respect to L_{GATE}; the same V_T and T_{OX} data are seen to be nearly proportional to V_{DD}.
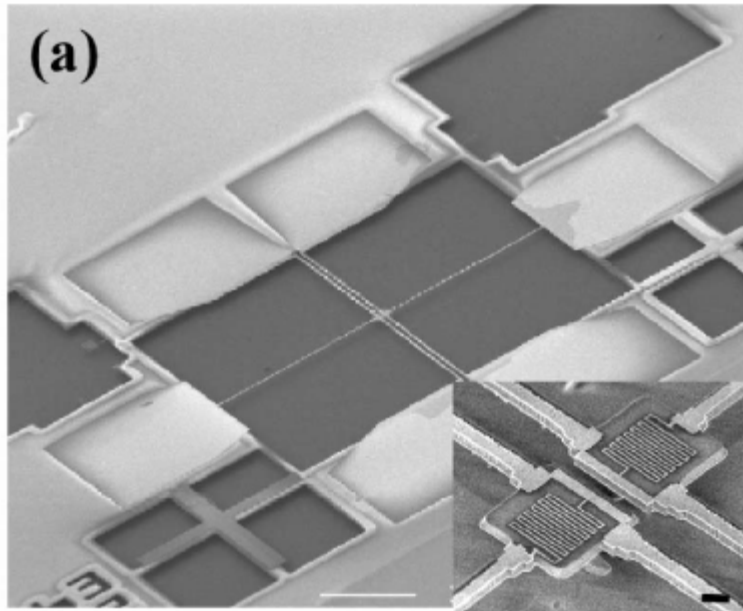
Nowak, IBM

$$\tau \cong \frac{2L_G^2 \times V_{DD}}{\mu\left(V_{DD} - V_T\right)^2}$$

$$P = C_G V_{DD}^2 f$$

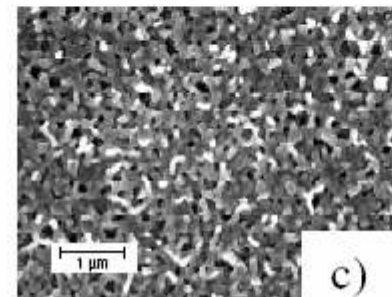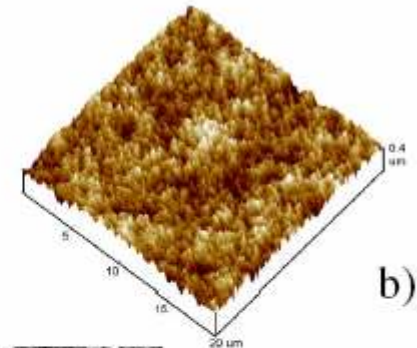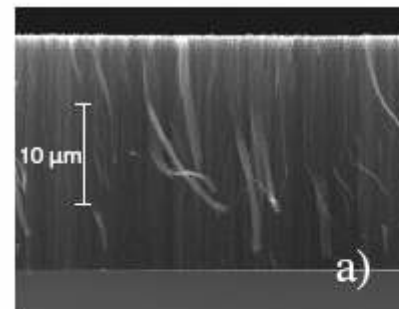- Classic scaling rule fails; passive power becomes a bigger issue.

Chuan Hu/Intel 2008

# Thermal solutions: CNT TIM/Diamond

P Kim, UC Berkeley, 2001

MWCNT: K=3000 W/mK

M Panzer, Stanford, 2006

SWCNT: R=0.12 cm^{2}K/W

- Improved thermal interface material, good intrinsic properties but complicated contact system, uncertain reliability. Still ways to go.
- Activities on chemical vapor deposited diamond CVDD: energy cost, polishing

Thermal solution: TEC/refrigeration
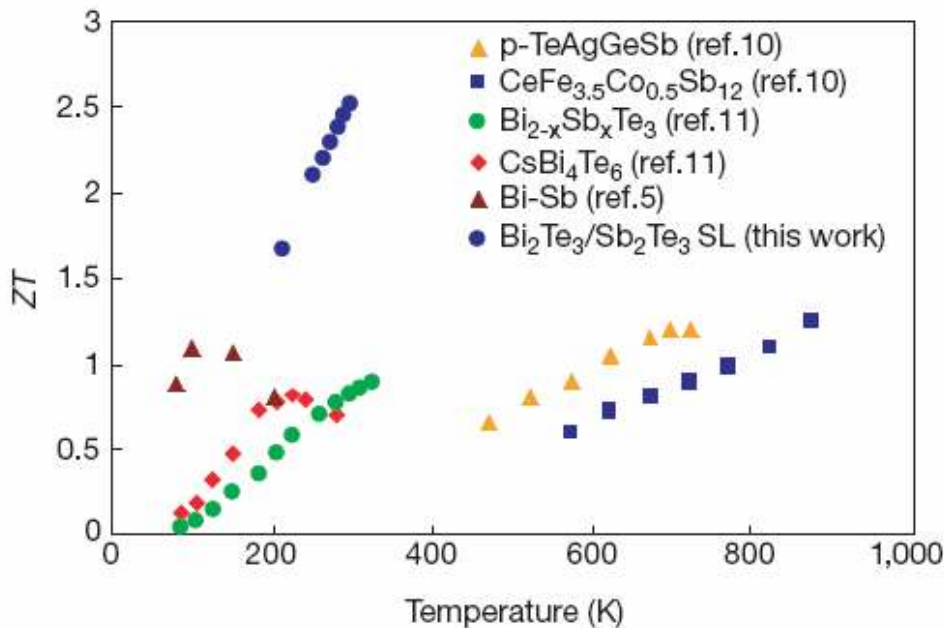
Figure 3 Temperature dependence of ZT of 10Å/50Å p-type Bi_2Te_3/Sb_2Te_3 superlattice compared to those of several recently reported materials.
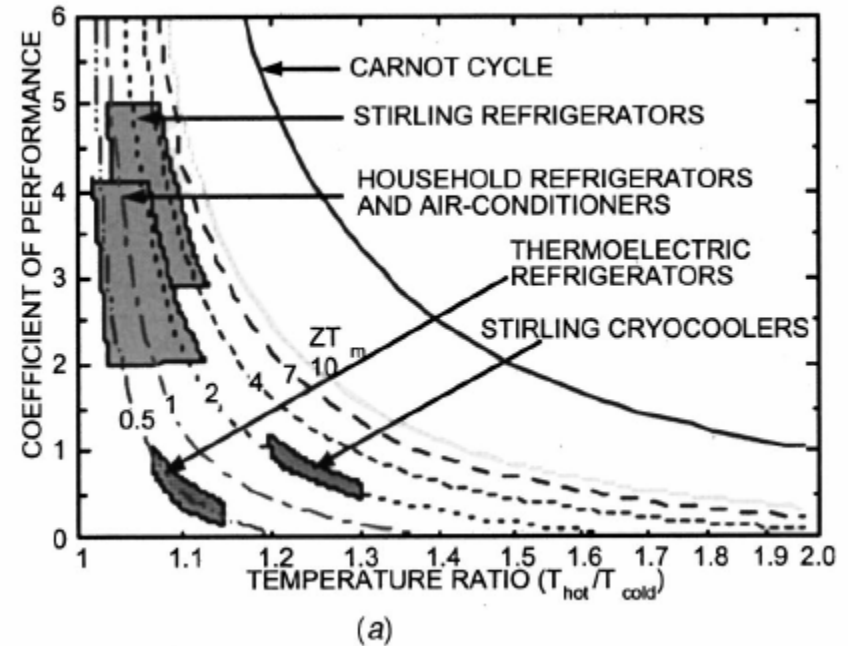
Rama V RTI 2001

Super lattice Be_2Te_3/Sb_2Te_3
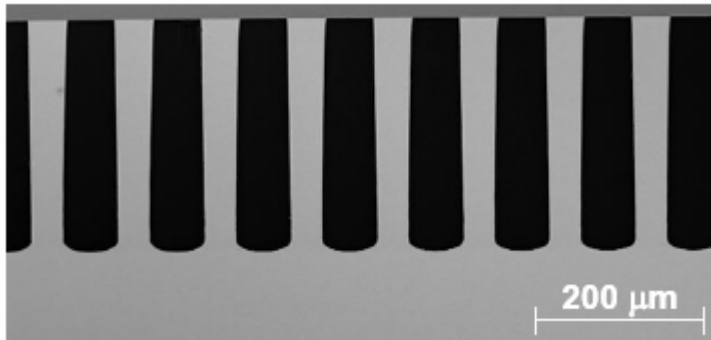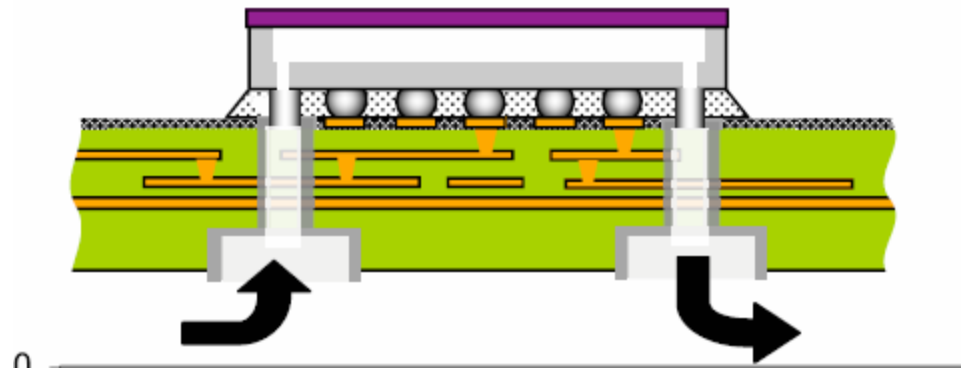

G Chen MIT 2002

Comparison of performance

- Solid state refrigeration with no moving parts. Supper lattice process is expensive. Other mechanisms limited success. Other refrigeration activities such as miniaturizing compressor, adsorb refrigerator. Form factor, efficiency and reliability concerns.
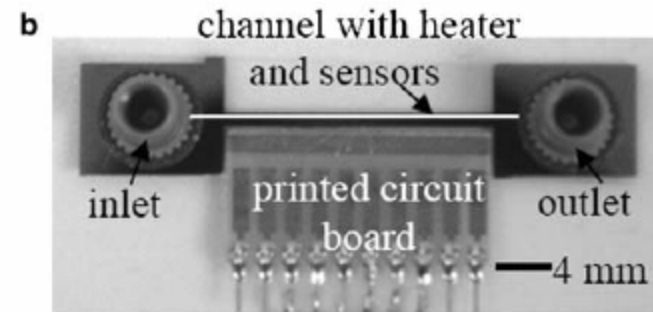
Thermal solution: liquid

Meindl, Georgia Tech. Single Phase

Chang, Intel

Single phase uchannel

Goodson, Stanford Phase change

- Microchannel has the best performance. Fabrication/pressure drop/compatibility/cost issues. Phase change microchannel has even less mass flow rate requirement.

Density: I

| Year of Production	2007	2008	2009	2010	2011	2012	2013	2014	2015
Bump pitch (µm)									
High density interconnect substrates	190	180	170	160	150	140	140	130	130
Build-up substrates	130	120	110	100	100	90	90	80	80
Coreless	130	120	110	100	100	90	90	80	80
Lines/space width (µm)									
Rigid Structure	35	30	30	25	25	22	22	20	20
Build-up substrates (core layer)	35	30	30	25	25	22	22	20	20
Build-up substrate (build-up layer)	15	10	10	10	9	8	8	6.8	6.4
Coreless	20	15	15	10	9	8	8	6.8	6.4
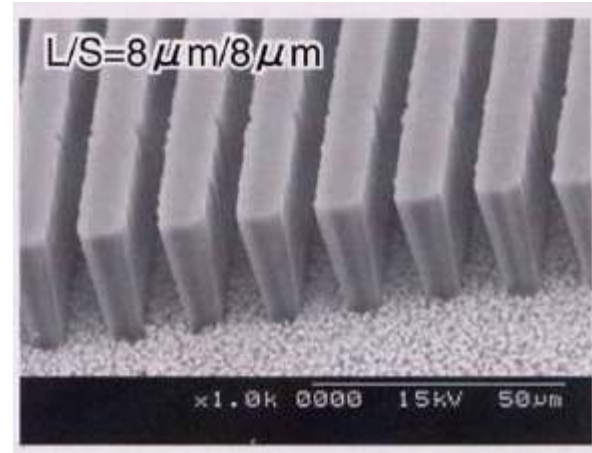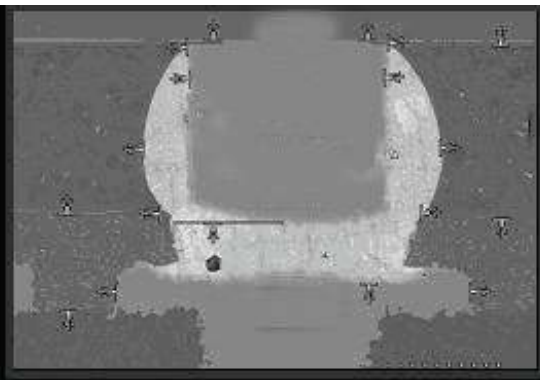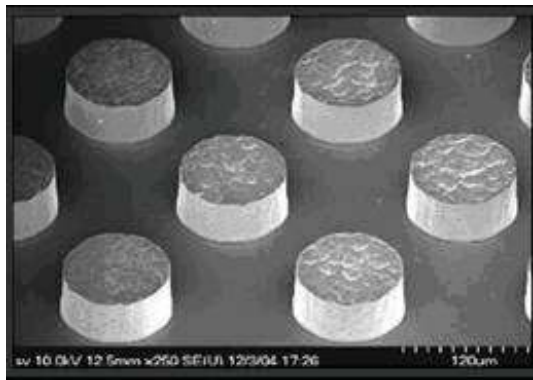
Flipchip bump pitch scaling: ITRS   Line/space scaling Hitachi, dry film

- Cost, enabling process, bandwidth,

Chuan Hu/Intel 2008

Density: II
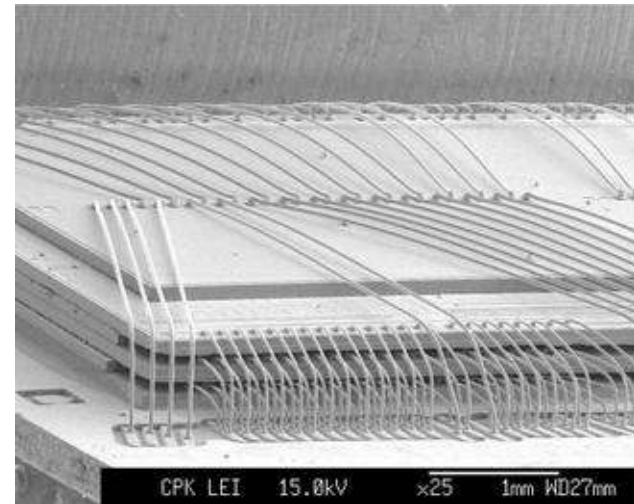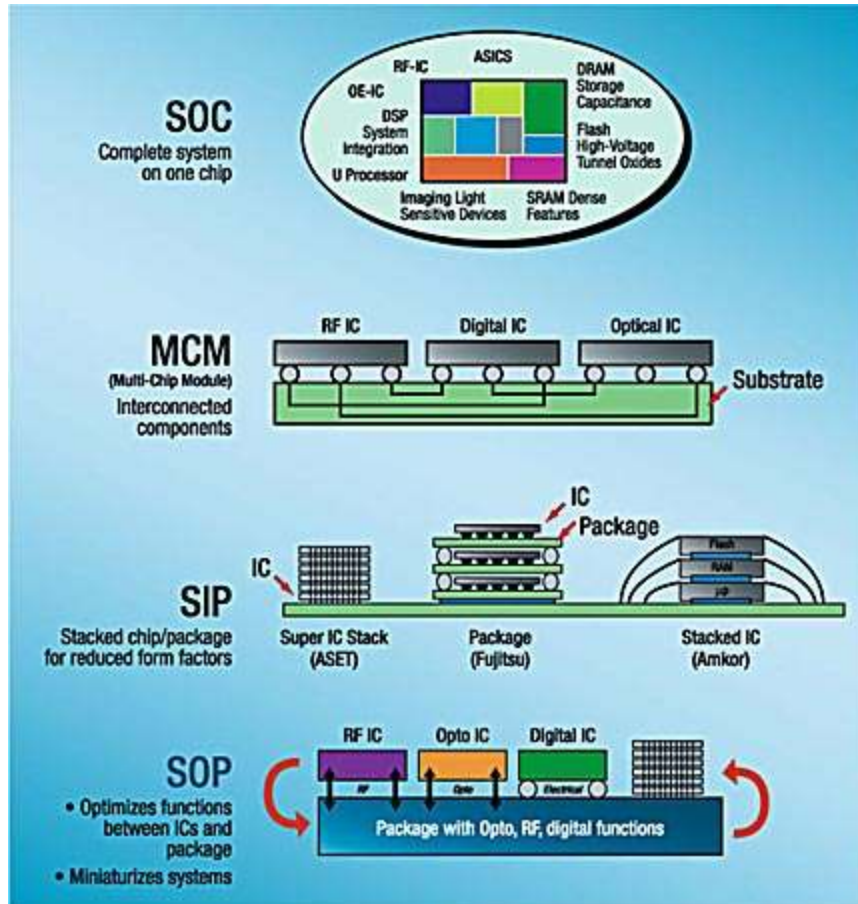
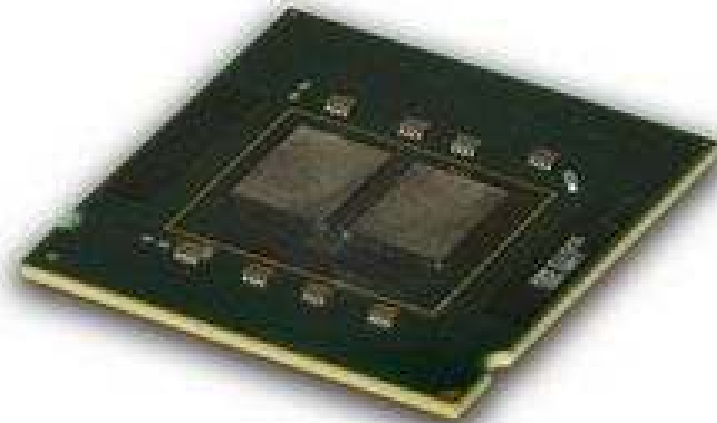
- SOP, SIP, SOC: many components with very different material properties and processing methods…

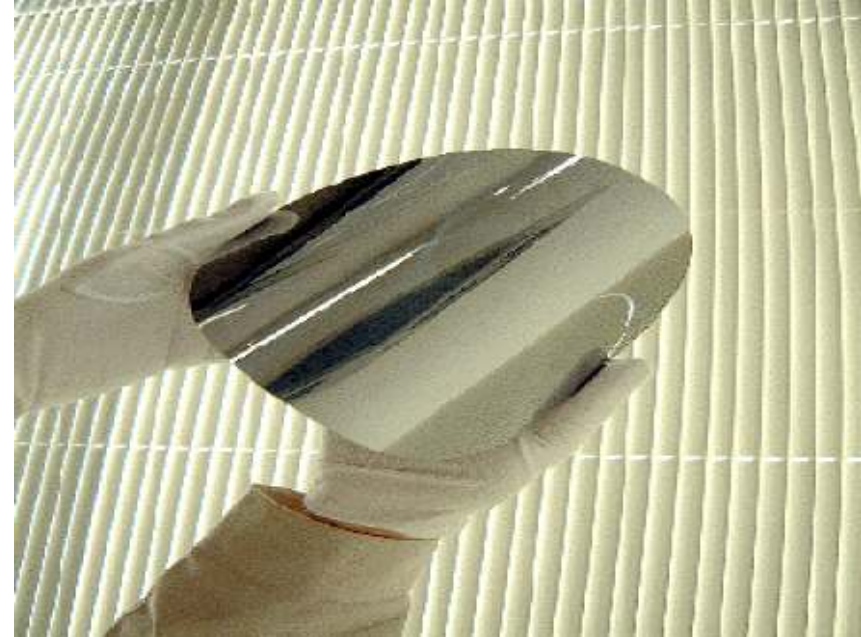# Multi Chip Module/Package

MCM IBM

MCP Intel

- Better yield, flexible design, better power dissipation/heat removal
- Interconnect among dies: Band width, substrate flatness/rigidity, cooling
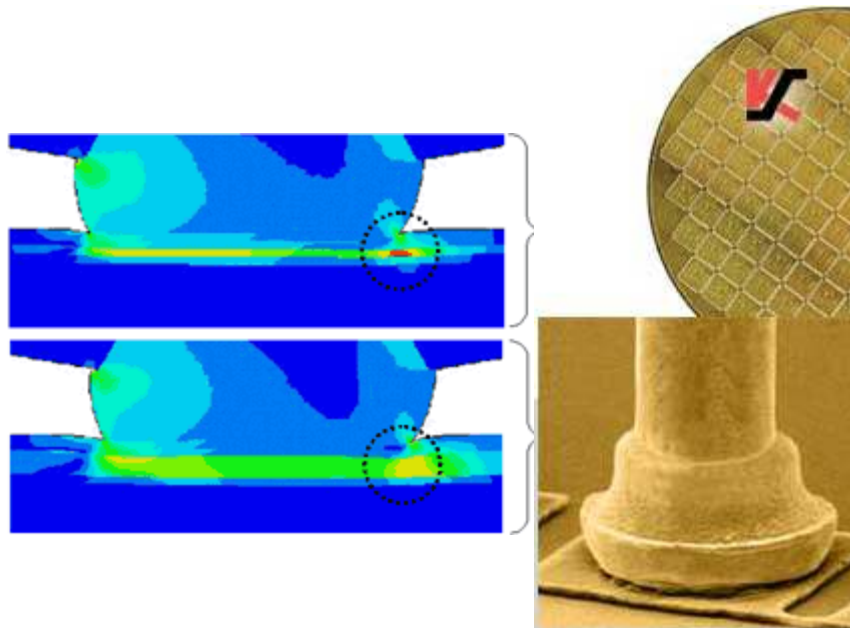
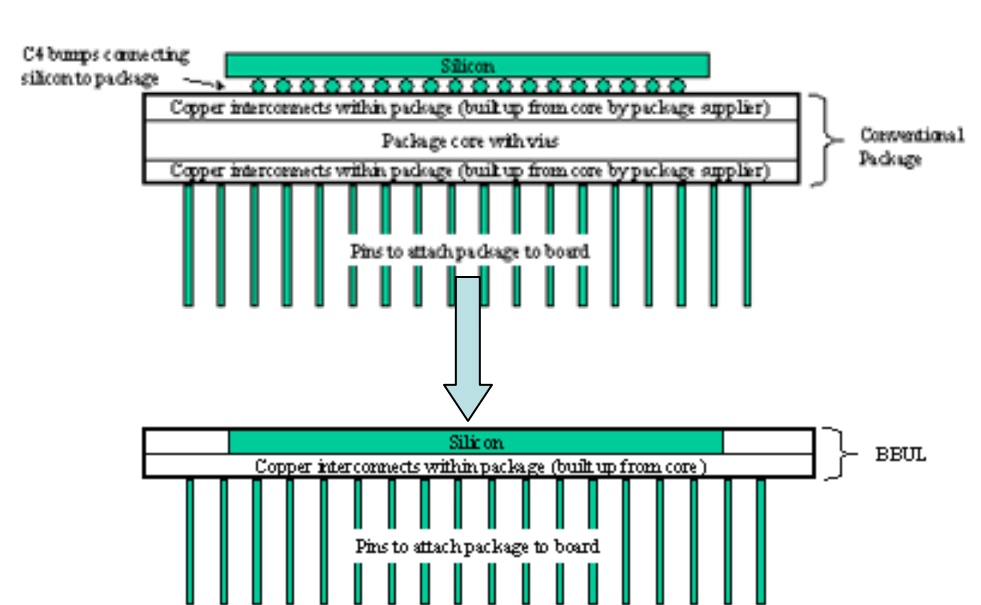# Form factor

Coreless substrate: NEC

Wafer thinning, 20 um Si: DISCO

- Coreless challenges: flatness, mechanical rigidity, assembly process
- Wafer thinning: contamination, compatibility with other processes, handling, flatness

Other packaging methods

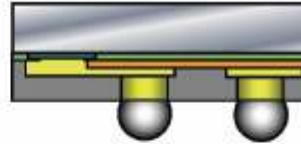Wire bonding: KSN

BBUL: bumpless buildup layer

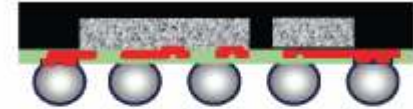- TSV, wire bonding (pressure vs. low k), BBUL (no C4,)

Wafer level packaging

Wafer level CSP in the simplest structure

Wafer level CSP with copper post and resin mold

Embedded wafer level ball grid array

Opto wafer level CSP with tapered TSV interconnection

Opto wafer level CSP with beam lead metallurgy
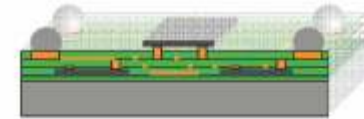
Thin chip integration (embedded device in polymer dielectric)

IPD embedded silicon substrate

Build-up substrate through wafer level fabrication
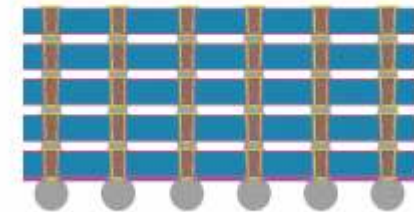
Stacked devices with Through Silicon Via's (TSVs)

ITRS 2007

- Broad family of processes for many different reasons: cost is one of them.

Chuan Hu/Intel 2008

25

Compatible with other advance processes

Figure 14. *Examples of one-level packaging of (RF-)MEMS devices.*

NanoMEMS research

- MEMS packaging: corrosion, hermetic, temperature sensitive, pressure…
- Spintronics: fundamental wave propagation…

IO/bandwidth
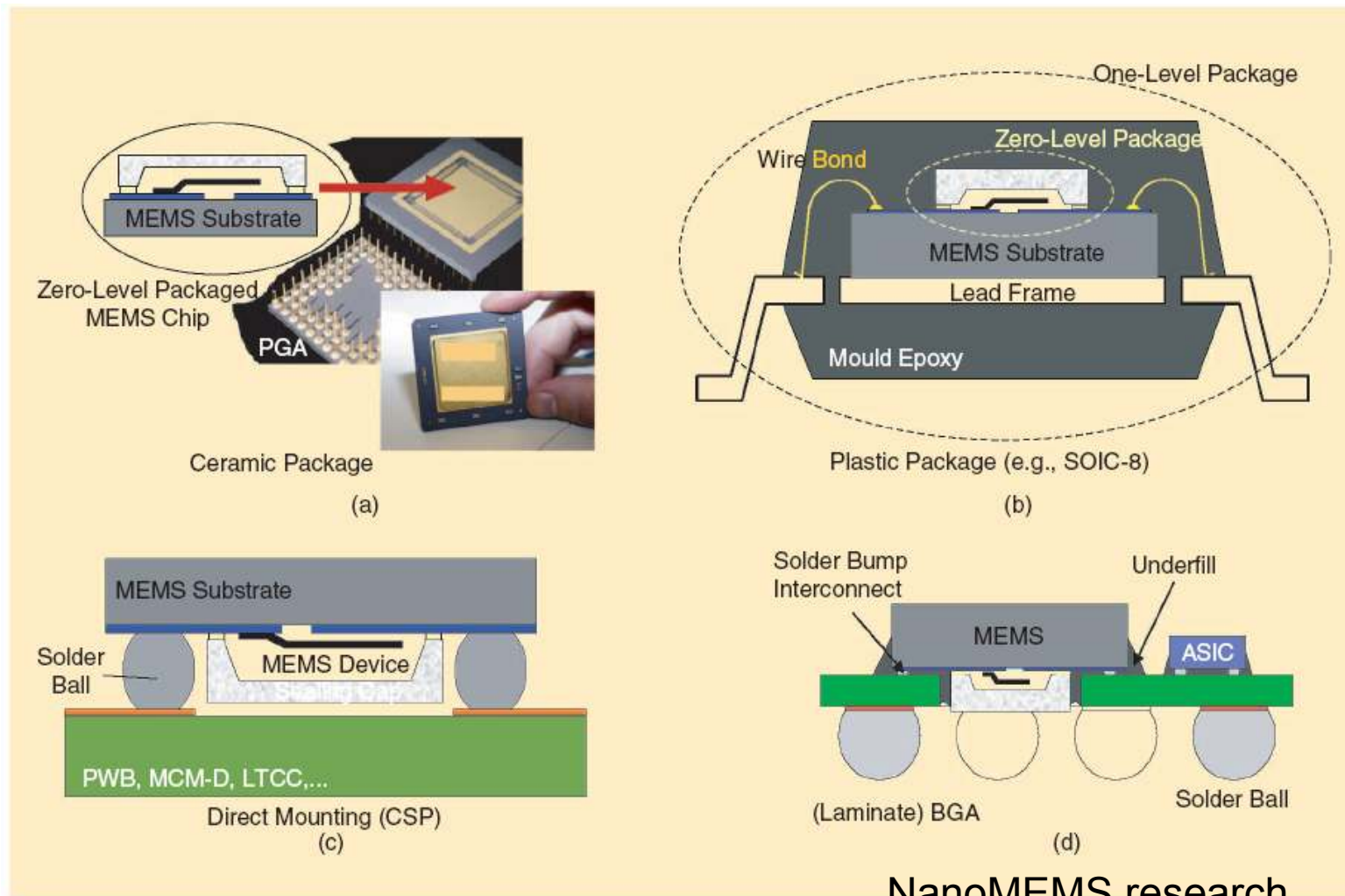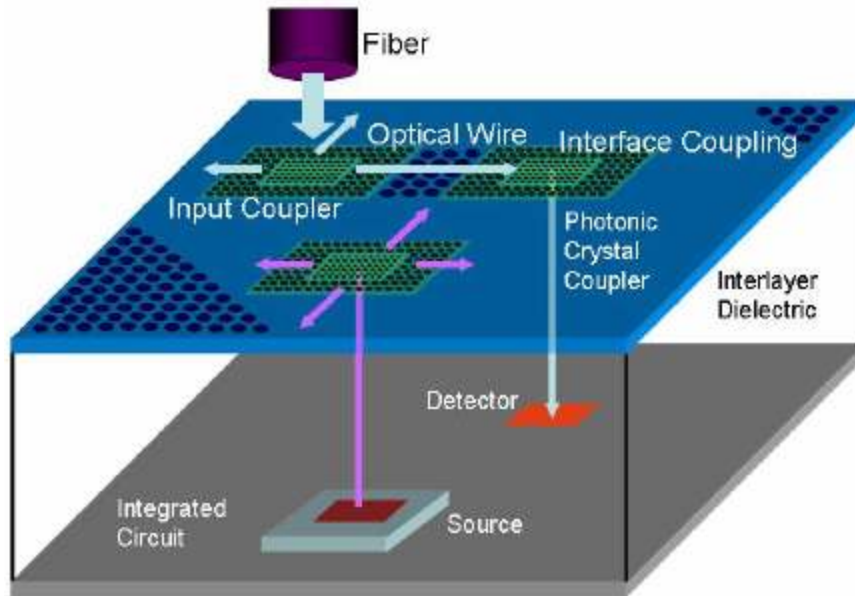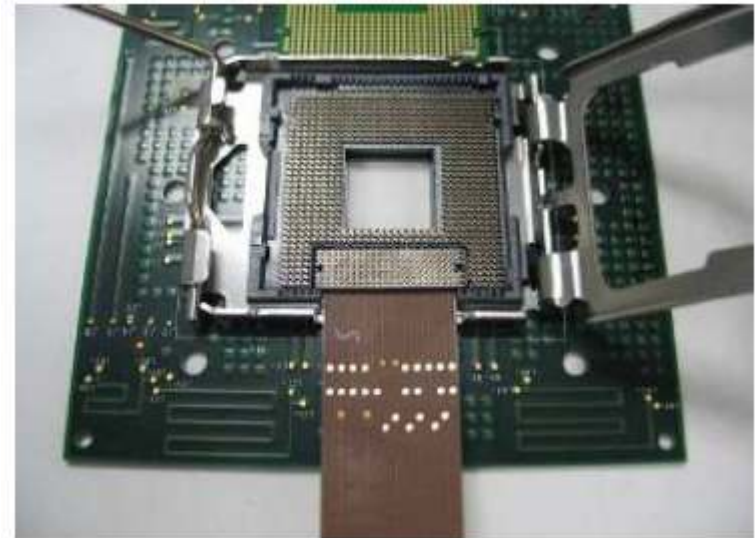

Opto-interconnect

Kolodziejsky MIT

Flex

Braunisch Intel

- Opto: High band width, distance? Si compatible solid state laser, waveguide,
- Flex: separate IO from power, power/bit issue

Environment

95Sn-5Ag
93.6Sn-4.7Ag-1.7Cu
96.2Sn-2.5Ag-0.8Cu-0.5Sb
65Sn-25Ag-10Sb
95.5Sn-3.5Ag-1.0Zn
95Sn-3.5Ag-1.0Zn-0.5Cu
91.8Sn-4.8Bi-3.4Ag
48Sn-46Bi-4Cu-2Ag
Bi 0.08-20%, Cu 0.02-1.5, Ag 0.01-1.5, P 0-0.20, rare earth mixture 0-0.20. balance Sn
91.0Sn-4.5Bi-3.5Ag-1.0Cu
67.8Sn-32.2Cd
99.3Sn-0.7Cu
99Sn-1Cu
97Sn-3Cu
95.5Sn-4Cu-0.5Ag
95.5Sn-3Cu-1Sb-0.5Ag

Leadfree solders: Indium.com

"Halogen-Free" Wiring Duct Drivers:

- **Fire Safety**
  - Smoke Toxicity
- **Fire Damage Prevention**
  - Prevent Corrosive Effects to Electronics
- **Higher Application Temperatures**
  - When higher temperature PVC products are not available
- **Environment**
  - Legislative Directives
  - Manufacturer "Green Product" Initiatives

Reason to go Halogen free

- Alternative choices don't have so impressive physical properties but we still have to change.

Chuan Hu/Intel 2008

Reliability

No-flow Underfill
Silicon Chip
Heated
Organic Substrate
Underfill Dispensing
Chip Placement
Solder Reflow & Underfill Cure

46 milliohms/sq < 17 milliohms/sq Direction of Electron Flow
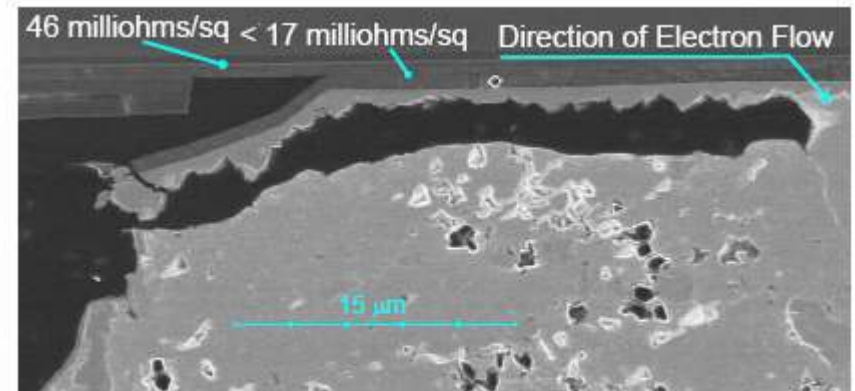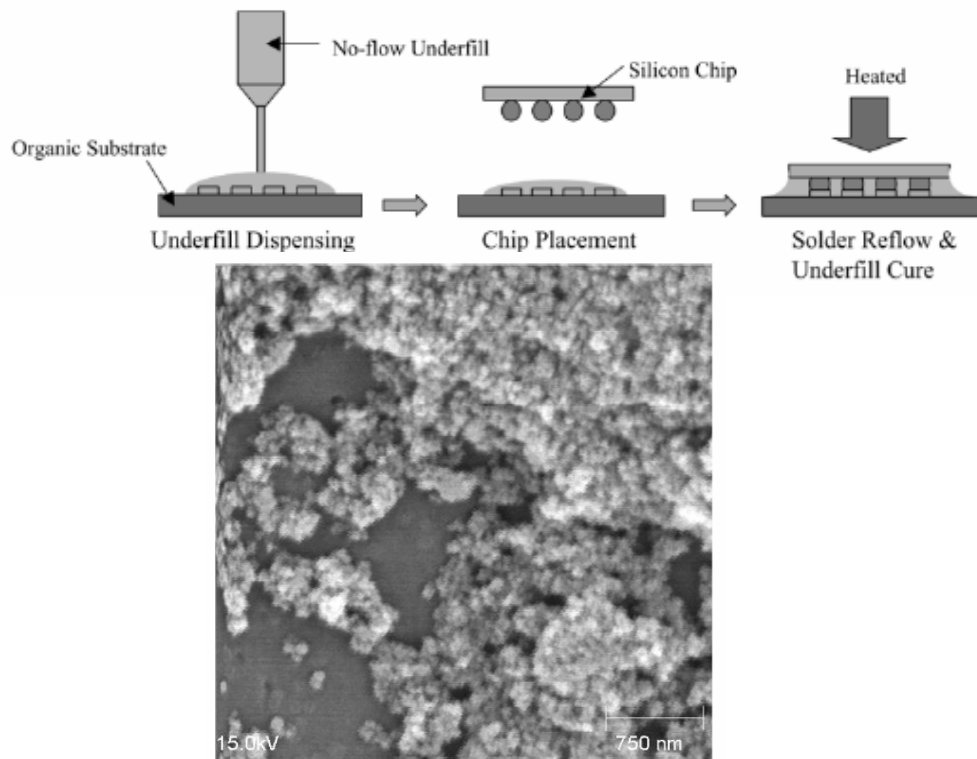
15 µm

15.0kV   750 nm

Figure 19   Added interconnect trace length (green arrow) due to void formation near the Die UBM metallization; Die 2, Bump 1.

Nano material underfill: for stress reduction

Wong, Georgia Tech

Electromigration

Tu, UCLA

- Higher current density, more complicated structures, high modulus and easier to reflow…

Cost

- Cost scaling is essential for the success of semiconductor industry.

Conclusion